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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,149	02/14/2002	Milivoje Aleksic	00100.02.0060(990060D-1)	7928
29153 7590 02/01/2008 ADVANCED MICRO DEVICES, INC. C/O VEDDER PRICE P.C. 222 N.LASALLE STREET CHICAGO, IL 60601			EXAMINER DANG, KHANH	
			ART UNIT 2111	PAPER NUMBER
			MAIL DATE 02/01/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/075,149

Applicant(s)

ALEKSIC ET AL.

Examiner

Khanh Dang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 November 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18-20, 24 and 25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 18-20, 24, and 25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

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DETAILED ACTION

Application Status

Applicants' RCE filed 11/13/2007 to continue prosecution of this application is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

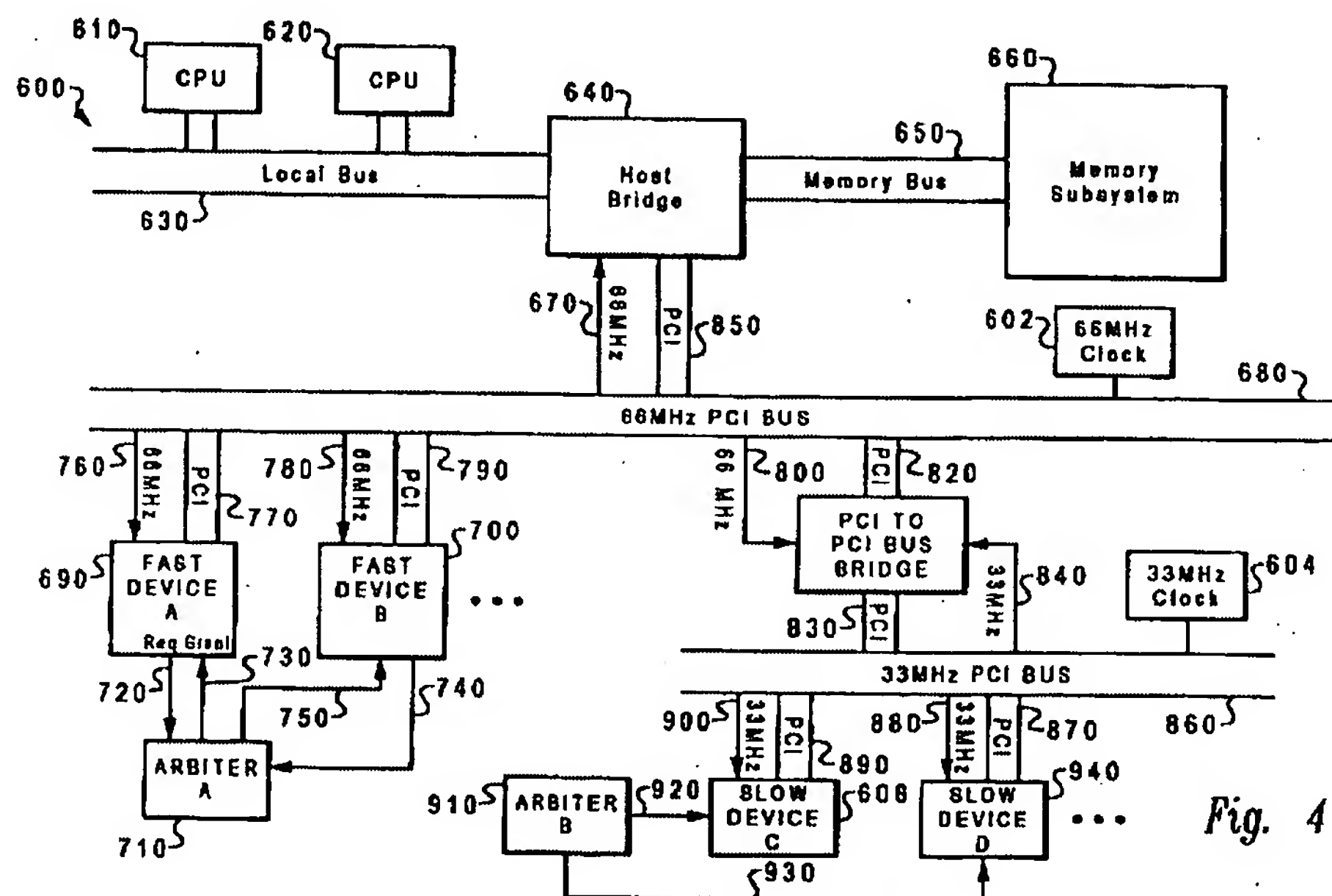
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 18-20, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iachetta Jr. (Iachetta, 5,727,171) in view of Porterfield and Ajanovic et al. (Ajanovic), and Heil et al. (Heil).

Iachetta discloses a data processing system as shown below in Fig. 4:

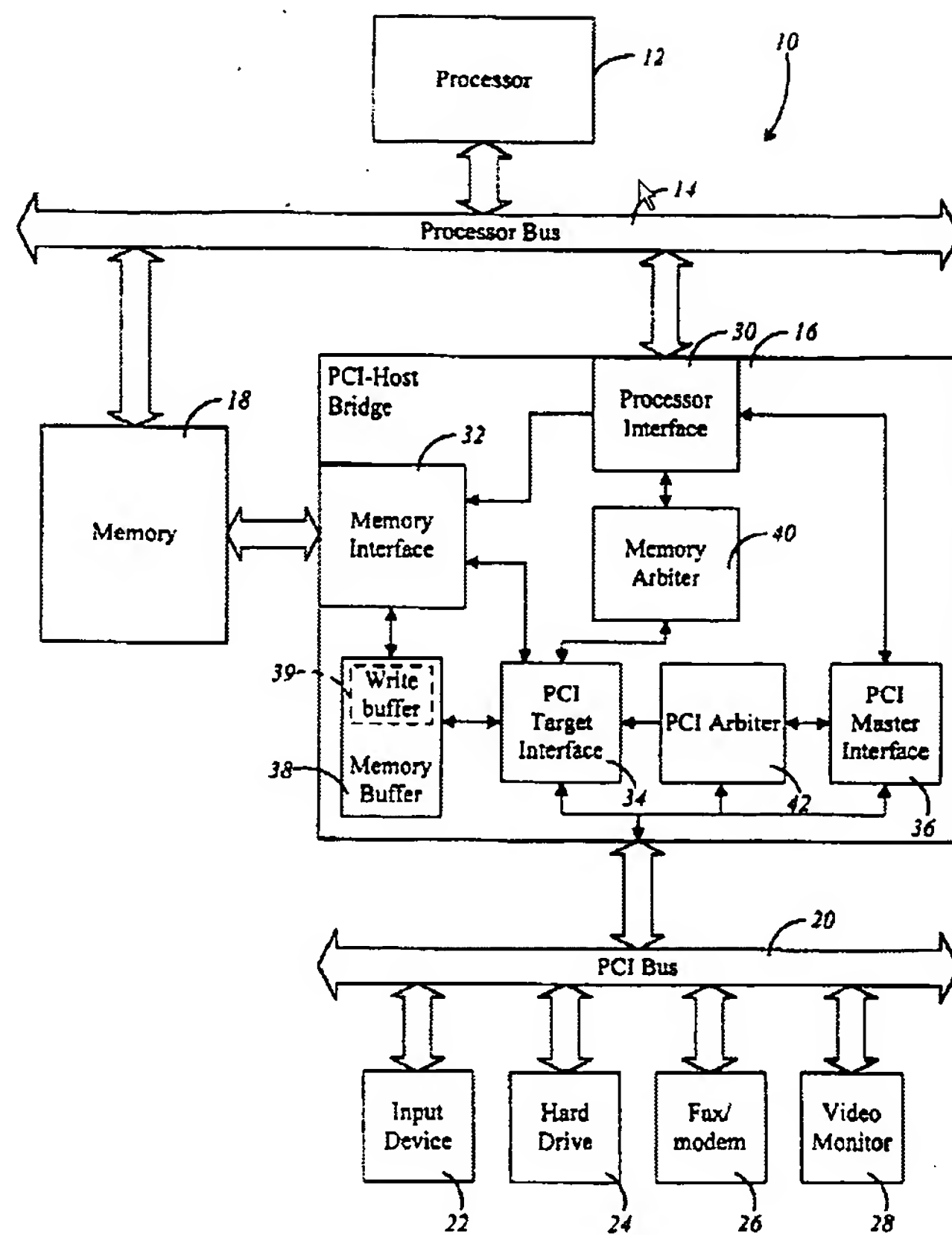


comprising:

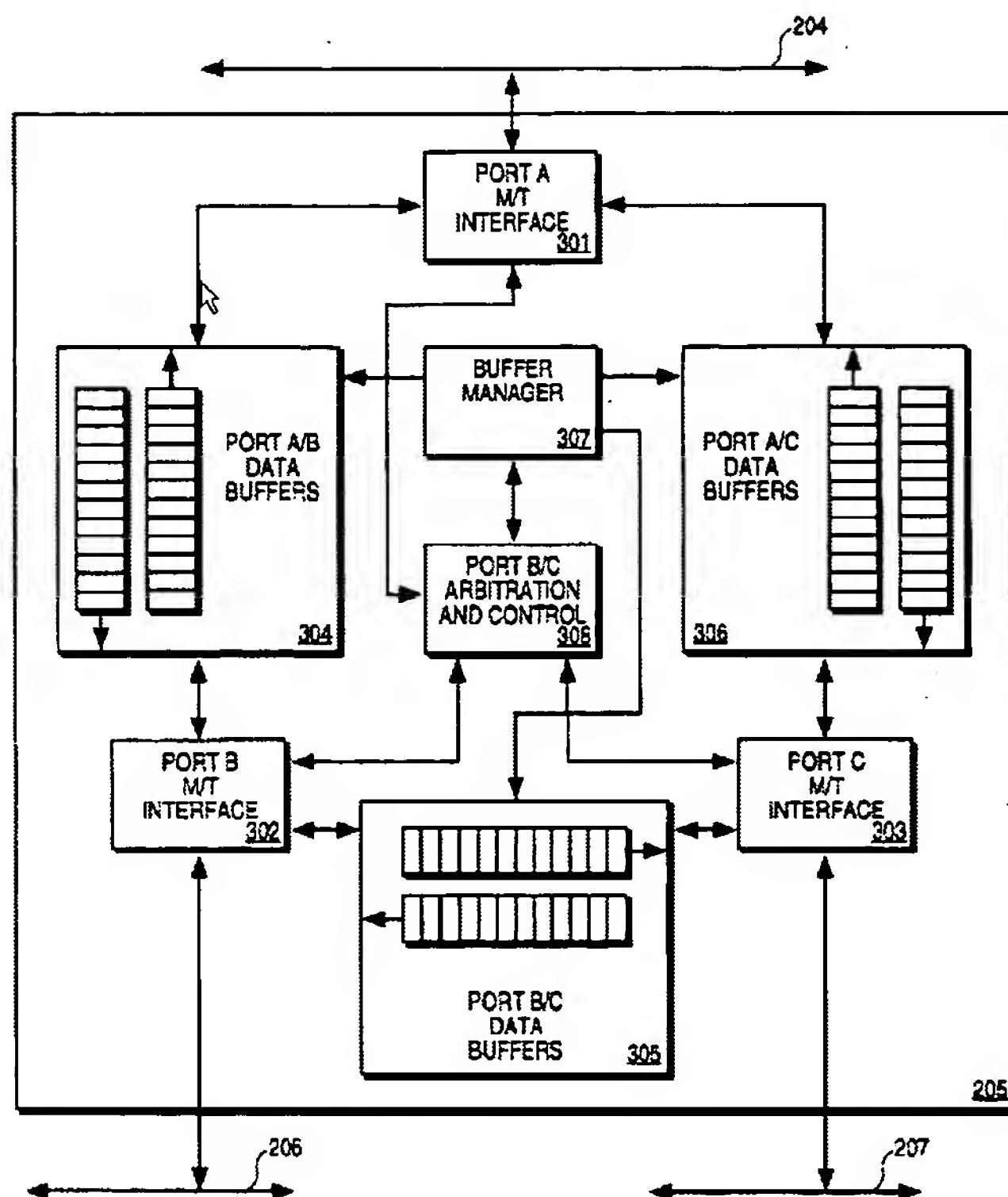
a system controller or host bridge 640 connected to memory 660 via a memory bus 650, a high speed arbiter 710 for providing arbitration to high speed devices A and B, an I/O controller or PCI/PCI bus bridge 810 coupled to a high speed bus 680, a low speed arbiter 910 for providing arbitration to low speed devices C and D; the PCI/PCI bridge 810, the fast devices A and B are all connected to high speed bus 680.

Izchetta does not disclose that the high speed arbiter may be included in the system controller or host bridge 640; and the low speed arbiter may be included in the I/O controller or PCI/PCI bridge 810.

However, the inclusion of an arbiter into the host bridge is old and well-known as evidenced by at least Porterfield. Porterfield disclose the use of an integrated arbiter 42 in a host bridge 16 as shown below:



Further, the inclusion of an arbiter into a PCI bridge 205 is also well-known as evidenced from Ajanovic. Ajanovic discloses an arbiter included in a PCI bridge 203:



Since all references are both from the same field of endeavor, the purpose disclosed by Porterfield and Ajanovic would have been recognized in the pertinent art of lachetta.

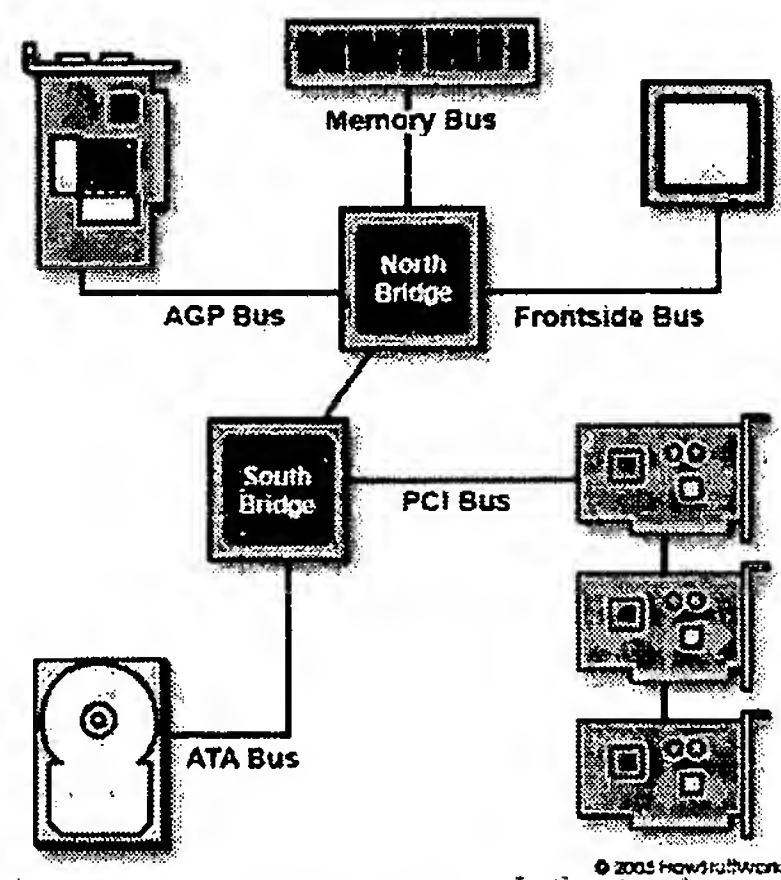
Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the high speed arbiter and low speed arbiter into the I/O controller or PCI bridge and system controller or host bridge, respectively, as taught by Porterfield and Ajanovic, for the purpose of reducing the number of discrete components, and thus, reducing cost; and also facilitating system integration. It is important to note that since the PCI bridge, the high speed devices A and B are all connected to the 66 Mhz high speed bus, it is clear only one device can access to the 66 Mhz bus at a time, and the high speed arbiter will provide arbitration to the PCI

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bridge, the high speed device A and the high speed device B for accessing the 66 Mhz high speed bus.

The further difference between the claim subject matter and lachetta is the use of dual channel memory controller. However, the use of dual channel memory controller, first developed by Intel, is old and well-known, as evidenced by at least Heil. Heil discloses a multiple-port structure. Heil discloses two separate memory channel controllers (figure 8, structures 134, 136, 142, and 144). Heil teaches that the general access latency caused by the severe bandwidth constraint can be improved with the dual memory channels (column 1, lines 52-56). Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Heil's teachings into lachetta for the purpose of improving the general access latency by the dual memory channels. Note also that it is inherent that a computer system, such as the system disclosed by lachetta must include a hard drive, and the hard drive is connected to the PCI bridge or PCI south bridge. See diagram below from How Motherboards Work, cited below. Note also that ATA Bus is operated as a higher speed than the low PCI Bus (33 Mhz).

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Note also that the memory bus 650 is not coupled to the low speed bus arbiter 910 and coupled to the storage device 660.

With regard to claim 24, see discussion above.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iachetta Jr. (Iachetta, 5,727,171) in view of Porterfield and Ajanovic et al. (Ajanovic), and Heil et al. (Heil) as applied to claims 18-20 above, and further in view of the following.

The further difference between the claim subject matter and that of Iachetta is the use of the integrated graphics engine into the host bridge or north bridge. However, the use of integrated graphics in the north bridge is old and well-known as evidenced by the definition of north bridge by Wikipedia cited below.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the graphics engine into the north or host bridge of Iachetta, since the use of integrated graphics in the north bridge is old and well-known.

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as evidence by the definition of north bridge by Wikipedia cited below, for the purpose of reducing the number of discrete components, and thus, reducing cost; and also facilitating system integration.

Response to Arguments

Applicants' arguments filed 11/13/2007 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris*, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997). As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112 Rejection:

Applicants' amendment to claim 18 overcomes the 112 Rejection.

The 103 Rejection:

Applicants argue that "Claim 18 requires, inter alia, that the input-output controller which is in communication with the high speed bus arbiter via the high speed bus, includes a low speed bus arbiter coupled to a low speed bus and also includes a separate bus that is instead coupled to a data storage device. Claim 24 also requires similar limitations in that the data storage device which is coupled to the I/O controller is coupled thereto via a different bus to transmit data at a higher rate than the data rate of the low speed bus arbiter which is in the I/O controller. As such, applicants respectfully submit that the claims are in condition for allowance. The lachetta reference suffers from the same problems as the prior art wherein the low speed arbiter is a bottleneck for the data going to the devices coupled to the low speed bus. The final office action does not appear to address this language regarding the I/O controller with separate bus and low speed arbiter and the cited portions of the referenced do not describe the claimed subject matter. Applicant respectfully submits that these claims are in condition for allowance."

Contrary to Applicants' argument, it is clear that when the high speed arbiter is incorporated into the Host Bridge, the high speed arbiter would become a high speed PCI bus arbiter. Thus, it is clear that the PCI/PCI bridge, connected to the Host Bridge (as in Fig. 4), is also connected to the PCI arbiter, which must be in full compliance

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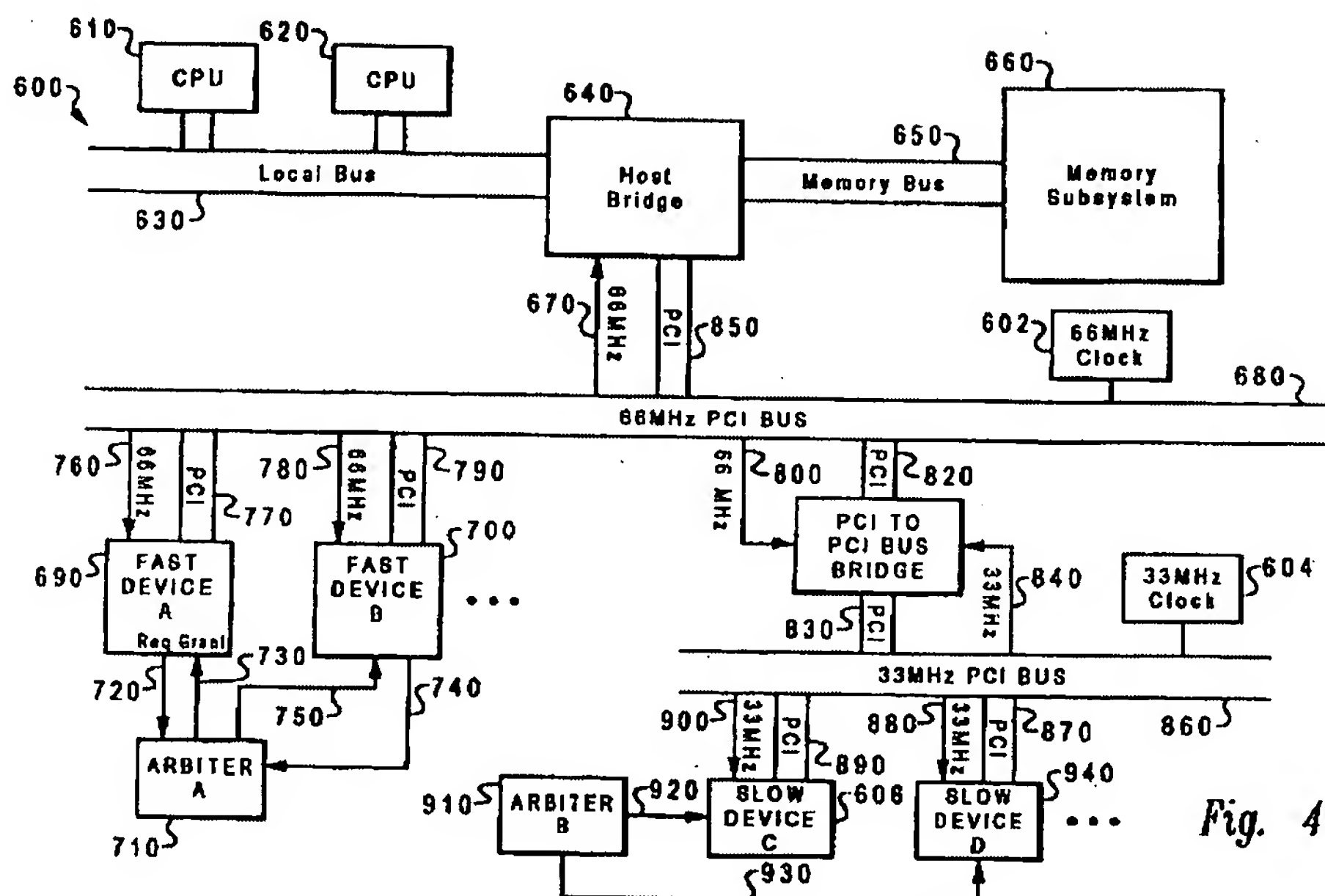
with the PCI specification. Note also that the PCI arbiter is included inside the Host Bridge. Note also that the word "coupled" does not mean a direct connection.

In any event, as disclosed by Iachetta, column 8, lines 28-51, reproduced below:

PCI to PCI bus bridge 810 is able to accomplish this task because it is connected to the same resources as both PCI bus 860 and PCI bus 680. PCI to PCI bus bridge 810 is
30 connected to PCI bus 680 by PCI connection 820. This connection contains the same data, address and control lines as does PCI connection 790 and PCI connection 770 which attach Fast Device B 700 and Fast Device A 690 to PCI bus
35 680. Also, PCI to PCI bus bridge 810 is connected to 66 MHz clock input 800. 66 MHz clock input 800 originates at the same source, 66 MHz clock source 602, as does the clock source for Fast Device A 690 and Fast Device B 700.

In a similar manner, PCI to PCI bus bridge 810 is
40 connected to PCI bus 860. PCI to PCI bus bridge 810 has a PCI connection 830 and a 33 MHz clock input 840. As it sees the same clock inputs and has the same connections to both PCI buses, PCI to PCI bus bridge 810 is able to read and write to both PCI bus 680 and PCI bus 860. The internal
45 circuitry of PCI to PCI bus Bridge 810 is then able to transmit data to and from both PCI buses even though both PCI buses run at different clock rates. This presents the advantage of allowing Fast Device A 690 and Fast Device B 700 to run at a faster clock rate than the Slow Device C 606 and Slow
50 Device D 940. These devices are allowed to run at a slower clock rate.

It is clear that the PCI connection 820 connecting the PCI/PCI bridge to the Host Bridge 640 via high speed PCI bus 680 and a single PCI connection 850, the PCI connections 770 and 790 connecting the high speed devices 690 and 700 to the Host Bridge via high speed PCI bus 680 and a single PCI connection 850, all contain the same data, address and control lines. The PCI connection 850 also contains data, address, and control lines used by the Host Bridge 640 to communicate with devices attached to the high speed bus 680. See column 7, lines 40-45. Fig. 4 is reproduced below:



Thus, it is clear that the high speed arbiter A, when incorporated into the Host Bridge 640, would become a PCI high speed bus arbiter for providing arbitration between all high speed devices including the PCI/PCI bridge 810 connected to the high speed PCI bus 680. In other words, the PCI high speed arbiter, which must be in full compliance with the PCI specification, is "coupled" to the PCI/PCI bridge 810 connected to the high speed PCI bus 680. Note that not only Porterfield teaches placing the arbiter into the Host Bridge, Iachetta, in the embodiment of Fig. 3, teaches that the high speed arbiter and the Host Bridge can be implemented in the same physical device. See Fig. 3, column 6, lines 33-37. Further, it is also clear that the memory bus 650 is not coupled to the low speed bus arbiter 910 and coupled to the storage device 660.

With regard to claim 25, Applicants argue that “Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Iachetta Jr. in view of Porterfield and

Ajanovic, and Heil et al. as applied to claims 18-20 above and further in view of 'Wikipedia cited below'. The claim requires a dual bus based unified memory architecture wherein a unified memory is controlled to store both graphics data and system data, in combination with other limitations and is at least allowable as depending on an allowable base claim."

Contrary to Applicants' argument, as already pointed out the previous Office Action, the use of integrated graphics in the host bridge/north bridge is old and well-known as evidence by the definition of north bridge by Wikipedia. Regarding the use of dual channel memory, as already discussed in the previous Office Action, the use of dual channel memory controller, first developed by Intel, is old and well-known. In case of integrated graphics (graphics controller provided with the Host Bridge/North bridge, and also known as on-board graphics), since the Host Bridge/North bridge is connected to the memory (with dual channel) via a memory bus, it is clear that the memory stores both "graphics data and system data."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Khanh Dang
Primary Examiner